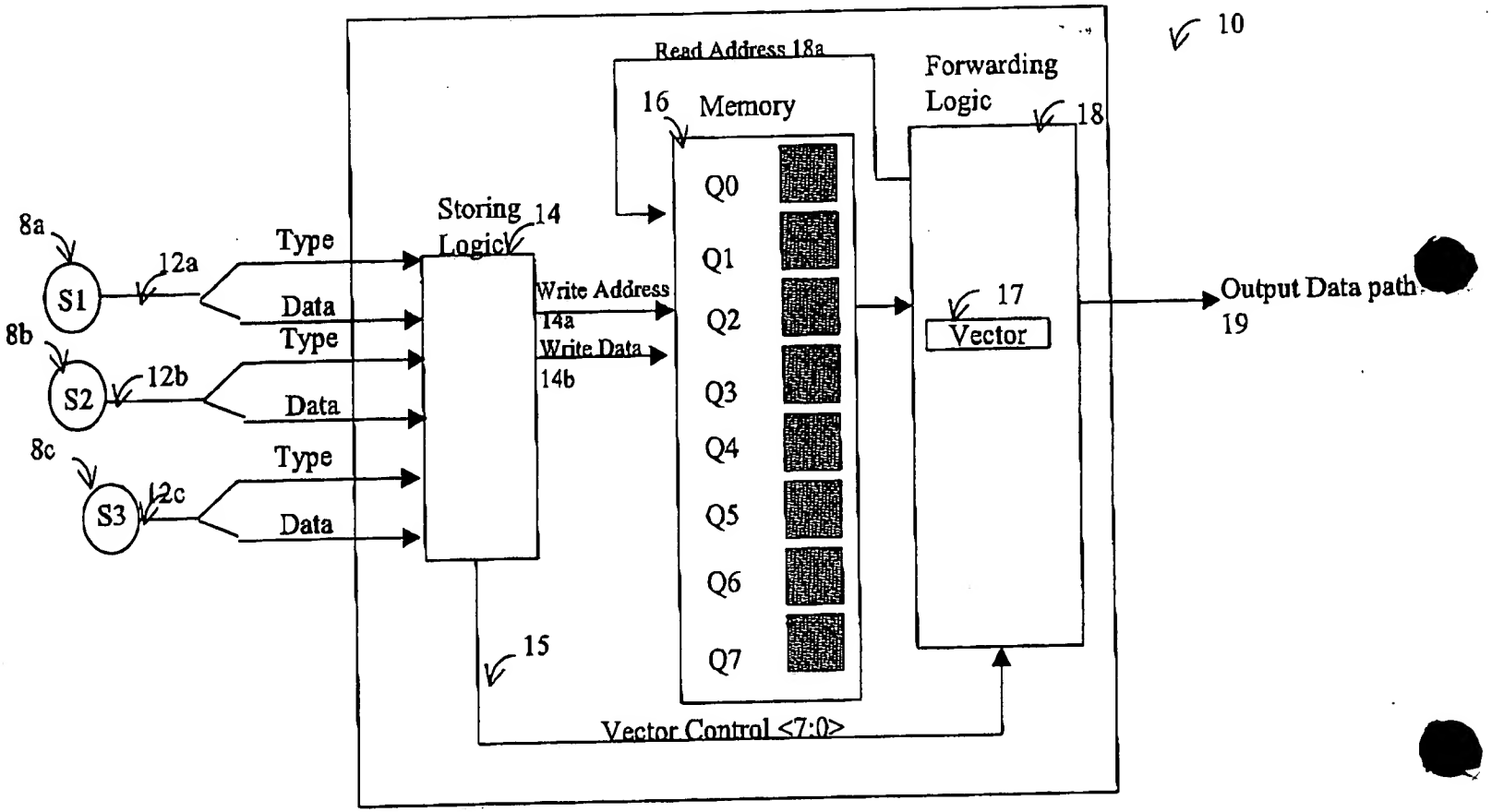
10
Read Address 18a
16 Memory
Forwarding Logic
18
8a
S1
12a
Type
Data
8b
S2
12b
Type
Data
8c
S3
12c
Type
Data
Storing Logic 14
Write Address 14a
Write Data 14b
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
17
Vector
Output Data path 19
15
Vector Control <7:0>

**Figure 1**

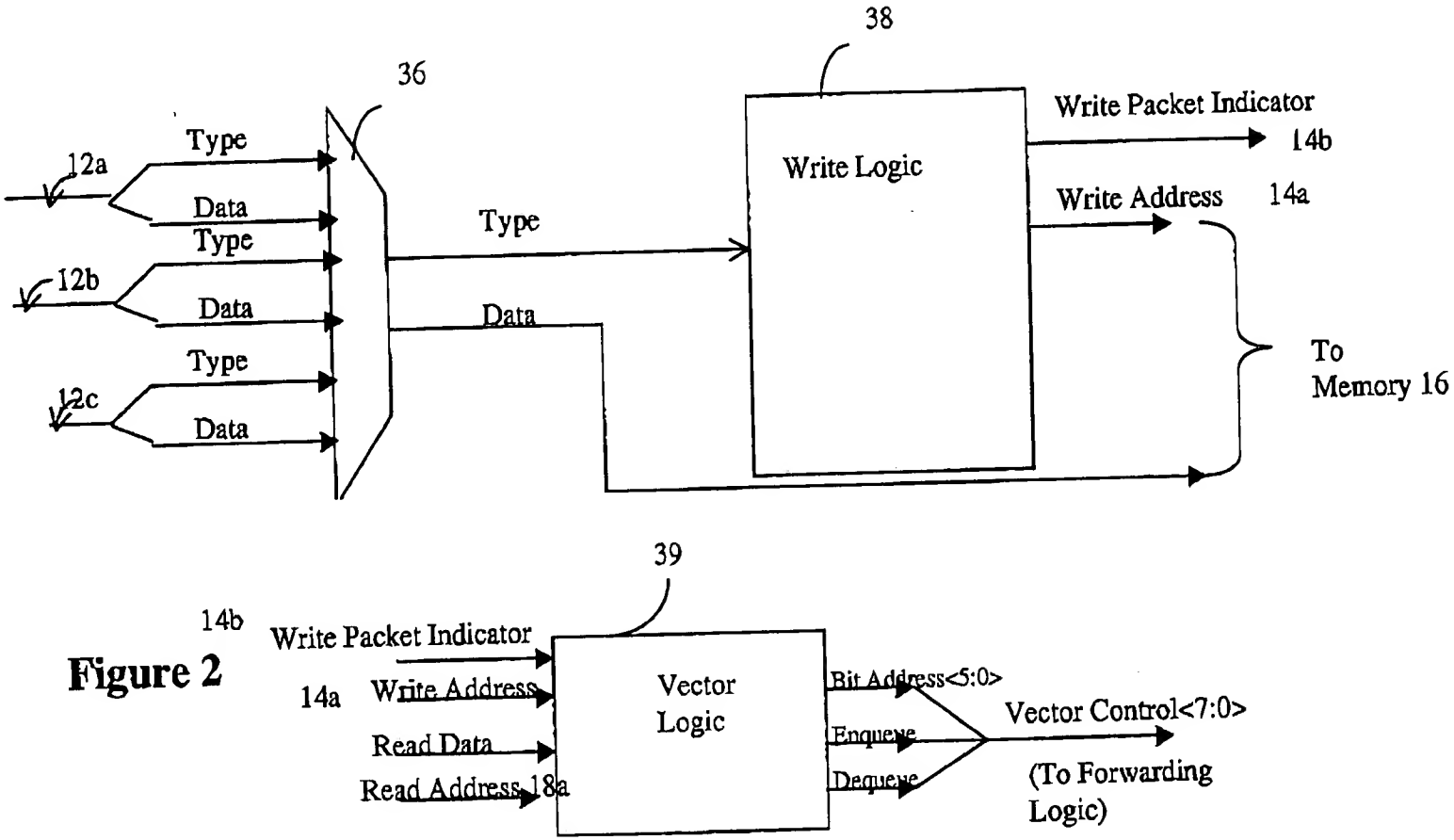
14
38
36
Write Logic
Write Packet Indicator
14b
Write Address
14a
Type
12a
Data
Type
12b
Data
Type
12c
Data
Type
Data
To
Memory 16
39
14b
Write Packet Indicator
14a
Write Address
Read Data
Read Address 18a
Vector
Logic
Bit Address<5:0>
Enqueue
Dequeue
Vector Control<7:0>
(To Forwarding
Logic)

**Figure 2**

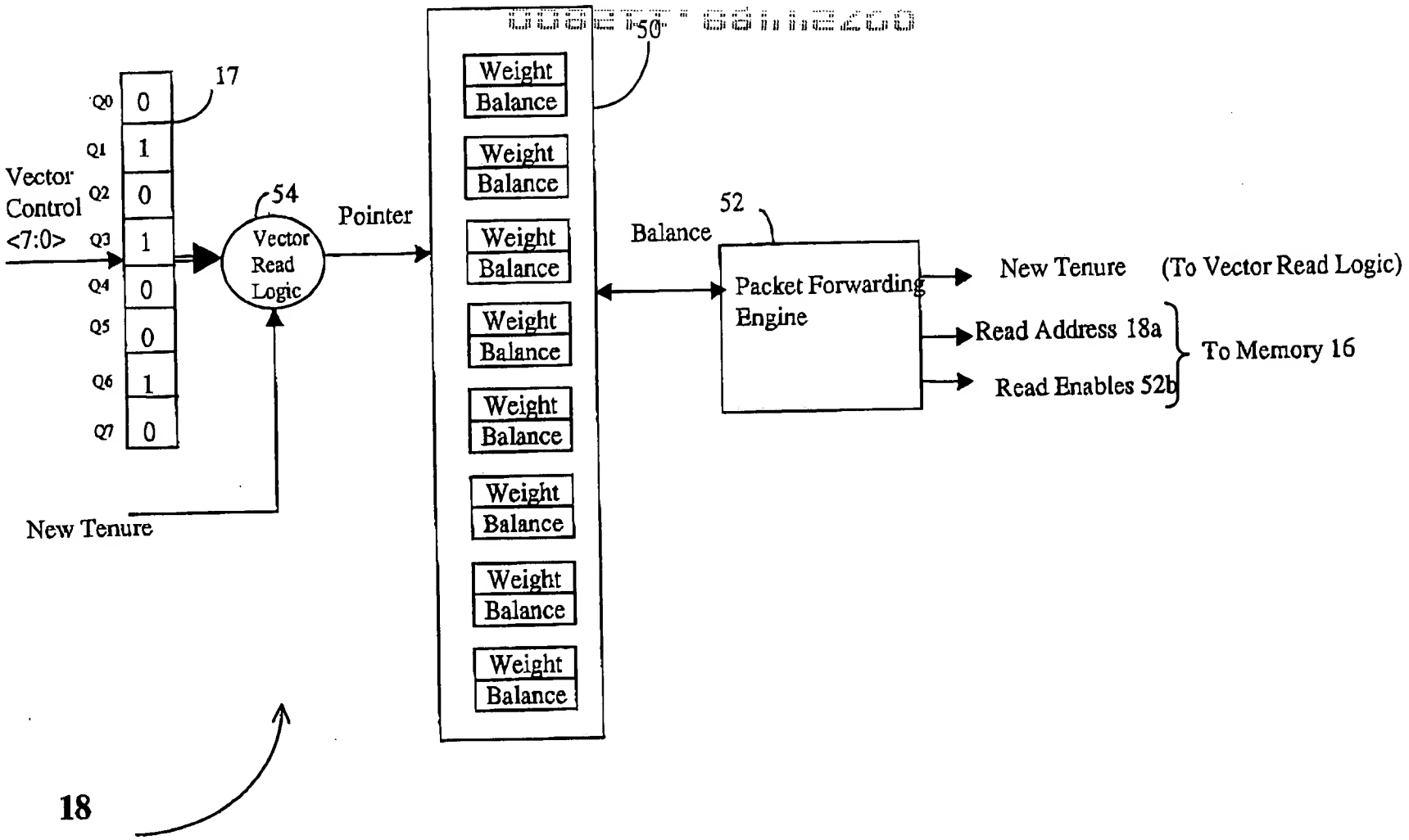
17
Q0 0
Q1 1
Q2 0
Q3 1
Q4 0
Q5 0
Q6 1
Q7 0
Vector Control <7:0>
54
Vector Read Logic
Pointer
New Tenure
50
Weight
Balance
52
Balance
Packet Forwarding Engine
New Tenure (To Vector Read Logic)
Read Address 18a
Read Enables 52b
To Memory 16
18

**Figure 3**

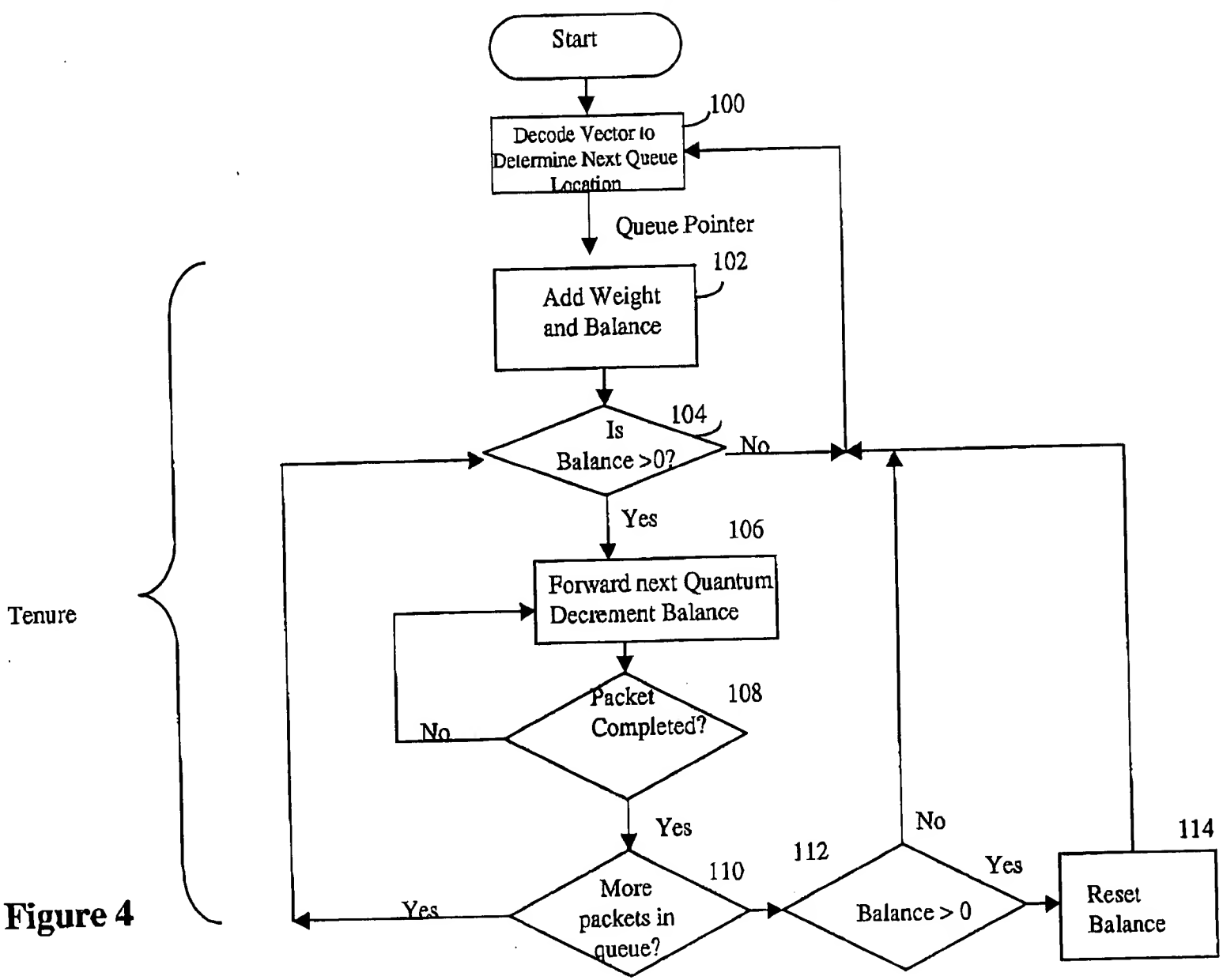
Start
Decode Vector to Determine Next Queue Location
100
Queue Pointer
Add Weight and Balance
102
Is Balance >0?
104
No
Yes
Forward next Quantum Decrement Balance
106
Packet Completed?
108
No
Yes
More packets in queue?
110
Yes
Balance > 0
112
No
Yes
Reset Balance
114
Tenure

**Figure 4**

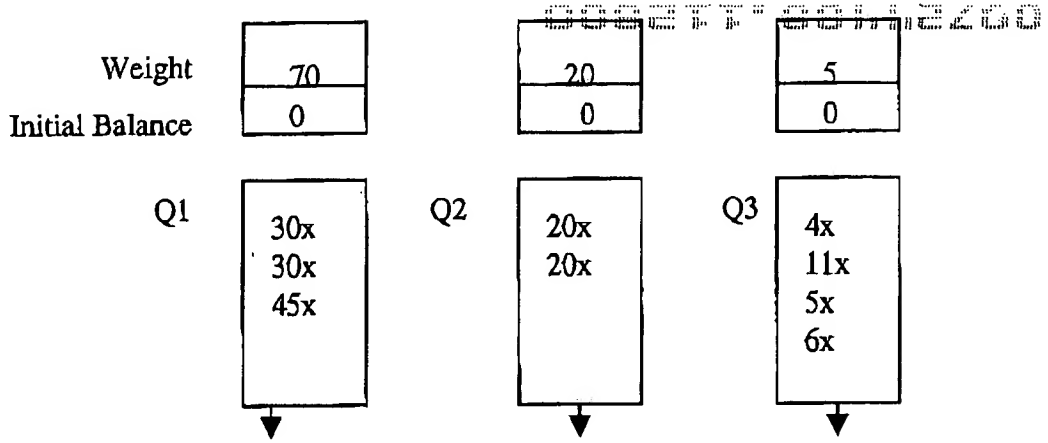


**Figure 5**

| | | | |
|---|---|---|---|
| 1st iteration | Balance = 70<br>45x<br>30x<br>Balance = -5 | Balance = 20<br>20x<br>Balance = 0 | Balance = 5<br>6x<br>Balance = -1 |
| 2nd iteration | Balance = 65<br>30x<br>Balance = 0 | Balance = 20<br>20x<br>Balance = 0 | Balance = 4<br>5x<br>Balance = -1 |
| 3rd iteration | Balance = 0 | Balance = 0 | Balance = 4<br>11x<br>Balance = -7 |
| 4rd iteration | Balance = 0 | Balance = 0 | Balance = -2 |